Serial No.: 10/675,432
Accompanying Amendment

Docket No. 1001.29
Customer No. 53953

REMARKS

Applicant respectfully requests reconsideration of this application in view of the following remarks. Claims 1-5, 8-15 and 18-20 have been amended. Claims 1-20 are pending. Antecedent basis for the amendments is located throughout Applicant's specification and the original claims, as for example in connection with the discussion of Figs. 3 and 4 at page 13, line 1 through page 16, line 22. Accordingly, no new matter has been entered.

Rejection of the claims

The Office Action rejected claims 1 and 11 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0210728 ("Flautner").

Claim 1 recites:

> 1.   A method of reducing power consumption in an N-way set-associative cache memory having Y sets, wherein N is a first integer, and wherein Y is a second integer, the method comprising:
>   during a first clock cycle k, in response to a first address, identifying a first associated set in the cache memory, comparing the first address to respective tag portions of N blocks in the first associated set, and outputting a first signal in response thereto, wherein k is an integer;
>   in response to the first signal indicating that one of the N blocks in the first associated set is a match with the first address, enabling a respective non-tag portion of the matching block in the first associated set;
>   during a second clock cycle $k+1$, in response to the first signal indicating that one of the N blocks in the first associated set is a match with the first address, reading the enabled non-tag portion of the matching block in the first associated set;
>   during the second clock cycle $k+1$, in response to a second address, identifying a second associated set in the cache memory, comparing the second address to respective tag portions of N blocks in the second associated set, and outputting a second signal in response thereto; and
>   in response to the second signal indicating that one of the N blocks in the second associated set is a match with the second address, enabling a respective non-tag portion of the matching block in the second associated set instead of the respective non-tag portion of the matching block in the first associated set.

Claim 11 recites:

11.   A system for reducing power consumption in an N-way set-associative cache memory having Y sets, wherein N is a first integer, and wherein Y is a second integer, the system comprising:

first circuitry for: during a first clock cycle k, in response to a first address, identifying a first associated set in the cache memory, comparing the first address to respective tag portions of N blocks in the first associated set, and outputting a first signal in response thereto, wherein k is an integer;

second circuitry for: in response to the first signal indicating that one of the N blocks in the first associated set is a match with the first address, enabling a respective non-tag portion of the matching block in the first associated set;

third circuitry for: during a second clock cycle $k+1$, in response to the first signal indicating that one of the N blocks in the first associated set is a match with the first address, reading the enabled non-tag portion of the matching block in the first associated set;

wherein the first circuitry is for: during the second clock cycle $k+1$, in response to a second address, identifying a second associated set in the cache memory, comparing the second address to respective tag portions of N blocks in the second associated set, and outputting a second signal in response thereto; and

wherein the second circuitry is for: in response to the second signal indicating that one of the N blocks in the second associated set is a match with the second address, enabling a respective non-tag portion of the matching block in the second associated set instead of the respective non-tag portion of the matching block in the first associated set.

In MPEP § 2131, the PTO provides that:

> "[t]o anticipate a claim, the reference must teach every
> element of the claim...."

Therefore, to sustain a rejection of claim 1, Flautner must contain all of the above-recited elements in claim 1. However, Flautner fails to teach the combination of elements in claim 1. In fact, the Office Action's cited portion of Flautner actually teaches away from such a combination.

Accordingly, Flautner fails to support a rejection of claim 1 under 35 U.S.C. § 102(e). In relation to claim 11, Flautner is likewise defective in supporting a rejection under 35 U.S.C. § 102(e).

Likewise, in relation to claim 1, Flautner is defective in supporting a prima facie case of obviousness. As between Flautner and Applicant's specification, only Applicant's

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specification teaches the combination of elements in claim 1. In fact, the Office Action's cited portion of Flautner actually teaches away from such a combination.

For example, at par. 112, Flautner states, "In order to assess the impact on performance of different control policies a number of test simulations were performed using alternative control policies. A first policy, denoted the 'simple policy' involves *periodically* resetting all lines in cache to drowsy mode. Here, *the period corresponds to the window size*. Furthermore, in this case no per-line access history is used in determining which cache lines to set to drowsy mode. A second policy, denoted the 'noaccess policy' sets to drowsy mode *only* those lines that have *not* been accessed within a given *update window*" (emphasis added). Further, at par. 114, Flautner states, "The graphs plot the percentage of drowsy cache lines against the percentage run-time increase for *update window sizes of 500, 2000, 8000, 32000 and 128000 cycles*" (emphasis added).

Accordingly, such control policies (e.g., with window sizes of 500, 2000, 8000, 32000 and 128000 cycles) are contrary to the element in claim 1 of "*in response to the second signal indicating that one of the N blocks in the second associated set is a match with the second address*, enabling a respective non-tag portion of the matching block in the second associated set *instead of* the respective non-tag portion of the matching block in the first associated set" (emphasis added). Consequently, Flautner teaches away from the combination of elements in claim 1.

Accordingly, in relation to claim 1, the PTO's burden of factually supporting a prima facie case of obviousness has not been met. In relation to claim 11, Flautner is likewise defective in supporting a prima facie case of obviousness.

Thus, a rejection of claims 1 and 11 is not supported.

Conclusion

For these reasons, and for other reasons clearly apparent, Applicant respectfully requests allowance of claims 1 and 11.

Dependent claims 2-10 depend from and further limit claim 1 and therefore are allowable.

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Dependent claims 12-20 depend from and further limit claim 11 and therefore are allowable.

An early formal notice of allowance of claims 1-20 is requested.

To the extent that this Accompanying Amendment results in additional fees, the Commissioner is authorized to charge deposit account no. 50-3524.

Applicant has made an earnest attempt to place this case in condition for allowance. If any unresolved aspect remains, the Examiner is invited to call Applicant's attorney at the telephone number listed below.

Respectfully submitted,

Michael A. Davis, Jr.
Registration No. 35,488

Date: November 2, 2006
Davis Law Group, P.C.
6836 Bee Caves Road
Suite 220
Austin, Texas 78746
Telephone 512-306-8324
Facsimile 512-306-8374
Docket Number: 1001.29

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